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EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/598,355	Applicant(s) BASCERI ET AL.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on th cov r sh t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 51-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25, 51-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 3- 6, 8, 9, 11, 13-16, and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kunitomo et al. (US 6,235,572).

Regarding claims 1, 3-6, 8, 9, Kunitomo et al. discloses a capacitor sémiconductor structure for storing charges comprising: an insulator (61, a tantalum oxide layer); a single conductive layer (51) having a compound (ruthenium oxide RuO) including a trace amount of the first substance (ruthenium) and a second substance (oxygen) is formed by oxidized the ruthenium lower capacitor (54) during crystallization of the tantalum oxide layer (61) (Kunitomo et al.'s col.20 lines 63-67, col.21 lines 1-15). Kunitomo et al. further teaches that the morphology of the semiconductor structure remain stable during the crystallizing process. Kunitomo et al.'s Fig.19, Fig.26 and col.20, lines 26-62.

It is noted that the second compound in Kunitomo et al. is identical as the second compound in the claims (ruthenium oxide). So, the second substance (oxygen) in

Kunitomo et al. is inherently capable to prevent the oxygen (one substance of insulator layer) form the tantalum oxide (61).

Regarding claims 11, 13, 16, and 18 , Kunitomo et al. teaches that the lower capacitor electrode (54) being formed from the conductive layer (51, a ruthenium oxide RuO layer) before forming the insulator layer (61), therefore the lower electrode have been already oxidized when performing the high temperature crystallization processing of the tantalum oxide (61); the further oxidation of lower electrode is restricted and the leakage current of the tantalum oxide can be reduce. Kunitomo et al.'s col.21, lines 23-34.

It is noted that, the tantalum oxide having a permittivity value greater than about 25. See references US5177570, US5463483 and US5814539 which were cited to support the fact that tantalum oxide having a permittivity value greater than about 25.

Regarding claim 14, the crystallization processing of tantalum oxide layer is under a condition at temperature of 650 to 850 degrees Celsius (noted that a range 750 to 801 is in a range of 650 to 850). Kunitomo et al.'s col.19, lines 1-14.

Regarding claim 15, as discussed in the rejection of claim 11, the ruthenium oxide passivates the tantalum oxide from undesired oxidation of lower capacitor electrode layer (54).

The limitation "as-deposited state" in claim 1 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps

which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Claims 16, 17, 19 and 20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Lin et al. (US 6,249,040).

Regarding claims 16, 19, Lin et al. discloses a capacitor semiconductor structure for storing charges comprising: an insulator layer (66) having a crystalline structure of substantially (001) lattice plane and a permittivity greater than 25 (Lin et al.'s col.7, lines 58-65); a conductive layer (69, an upper capacitor electrode having a single layer of Pt. col.8 line 9) formed on the insulator layer (66). See Lin et al.'s Fig.9H.

Regarding claim 17, Lin et al. teaches that the insulator layer (66) is a Ta2O5 (a ditantalum pentaoxide layer). Lin et al.'s col.7, lines 58-65.

Regarding claim 20, as above the insulator layer (66) having lattice plane of (001) that means the lattice plan of insulator layer is parallel to a-axis and b-axis and intersecting of c-axis (a=0, b=0, c=1).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,249,040) in view of Summerfelt et al. (US 5,622,893).

Regarding claims 16, 18, 19, Lin et al. discloses a capacitor semiconductor structure for storing charges comprising: an insulator layer (66) having a crystalline structure of substantially (001) lattice plane and a permittivity greater than 25 (Lin et al.'s col.7, lines 58-65); a conductive layer (69, an upper capacitor electrode having a uniform material of Pt. col.8 line 9) formed on the insulator layer (66). See Lin et al.'s Fig.9H.

Lin et al. does not teach that the upper capacitor (69) is formed of RuOx.

Summerfelt et al. discloses a capacitor structure comprising an upper capacitor electrode (40) formed of Pt or RuO2. See Summerfelt et al.'s Fig.9 and TABLE.

It would have been obvious to one of ordinary skill in the art to form upper electrode of RuOx (x=2) instead of Pt as taught by Summerfelt et al. into Lin et al.'s device because Pt and RuO2 are commonly used to form upper capacitor electrode and they are interchangeable. Both Pt and RuO2 are commonly used to form upper capacitor electrode because they are stable when contact to high dielectric constant capacitor insulating layer.

It is noted that the device formed by the combination of Lin et al. and Summerfelt et al. having the upper electrode layer(the conductive layer) formed of RuOx (x=2) which is the same material for forming the conductive layer as claimed. Therefore, the RuO2 conductive layer inherently mitigates the diffusion as claimed.

Regarding claim 17, Lin et al. teaches that the insulator layer (66) is a Ta2O5 (a ditantalum pentaoxide layer). Lin et al.'s col.7, lines 58-65.

Regarding claim 20, as above the insulator layer (66) having lattice plane of (001) that means the lattice plan of insulator layer is parallel to a-axis and b-axis and intersecting of c-axis (a=0, b=0, c=1).

Regarding claims 18, Lin et al. teaches all the limitations of claims 16, 17, 19 and 20 as shown above, however Lin et al. does not teach that the upper capacitor (69) is formed of RuOx.

Summerfelt et al. discloses a capacitor structure comprising an upper capacitor electrode (40) formed of Pt or RuO2. See Summerfelt et al.'s Fig.9 and TABLE.

It would have been obvious to one of ordinary skill in the art to form upper electrode of RuOx (x=2) instead of Pt as taught by Summerfelt et al. into Lin et al.'s device because Pt and RuO2 are commonly used to form upper capacitor electrode and they are interchangeable. Both Pt and RuO2 are commonly used to form upper capacitor electrode because they are stable when contact to high dielectric constant capacitor insulating layer.

Regarding claims 21 and 23, Lin et al. teaches that the dielectric Ta2O5 layer (66) formed on a first electrode (65) (Lin et al.'s Fig.9H). Noted that, the device formed by the combination of Lin et al. and Summerfelt et al. having a second electrode (the upper capacitor electrode) formed of RuOx (x=2) including a first substance (ruthenium) and a second substance (oxygen).

Regarding claim 24, as discussed in the rejection of claims 21 and 23 above, the dielectric layer (66) having a first compound includes a first substance (Ta) and a second substance (oxygen), the second electrode having a second compound (RuOx) including a trace amount of third substance (ruthenium) and a substantial amount of fourth substance (oxygen).

It is noted that, the second electrode in the device formed by the combination of Lin et al. and Summerfelt et al. is formed of RuOx which is identical as material of second

electrode of claimed device. Therefore, it is inherent that RuOx prevent the diffusion of oxygen from the Ta2O5 layer.

Regarding claim 25, Lin et al. teaches that the first electrode (65) is formed of Ru. Lin et al.'s col.8, lines 1-4.

Claims 2, 10, and 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. view of Yeom et al. (US 6,066,540).

Kunitomo et al. teaches all the limitations of claims 1, 3-4, 6, 8-9, 11, and 14-15 as shown above, however Kunitomo et al. does not explicitly teach that the tantalum oxide is a ditantalum pentaoxide layer.

Yeom et al. discloses a capacitor structure comprising a capacitor dielectric layer formed a tantalum oxide layer such as Ta2O5 (ditantalum pentaoxide). See Yeom et al.'s col.1, lines 37-40.

It would have been obvious to one of ordinary skill in the art to form tantalum oxide capacitor dielectric layer of ditantalum pentaoxide layer as taught by Yeom et al. in Kunitomo et al.'s device because tantalum oxide such as Ta2O5 having high permittivity. One of ordinary skill in the art would have been motivated to do so in order to increase the electrostatic capacity of the capacitor. Yeom et al.'s col.1, lines 27-40.

Claims 5, 7, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. view of Choi (US 5,702,970).

Kunitomo et al. teaches all the limitations of claims 1, 3-4, 6, 8-9, 11, and 14-15 as shown above, however Kunitomo et al. does not explicitly teach that the ruthenium oxide having a chemical formula as RuOx, where x is indicative of a desired number of atoms.

Choi discloses a capacitor structure comprising a lower electrode (15) is formed of ruthenium oxide (RuOx where x=2). See Choi's Fig.2G.

It would have been obvious to one of ordinary skill in the art to form ruthenium oxide capacitor lower electrode of RuOx as taught by Choi in Kunitomo et al.'s device because ruthenium oxide such as RuOx is stable under the heat treatment during the process of forming the capacitor dielectric layer. Choi's col.1, lines 40-50.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. view of Yeom et al. and further in view of Choi (US 5,702,970).

Kunitomo et al. and choi teaches all the limitations of claims 1-4 , 6, 8-12, and 14-15 as shown above, however Kunitomo et al. and Yeom et al. do not explicitly teach that the ruthenium oxide having a chemical formula as RuOx, where x is indicative of a desired number of atoms.

Choi discloses a capacitor structure comprising a lower electrode (15) is formed of ruthenium oxide (RuOx where x=2). See Choi's Fig.2G.

It would have been obvious to one of ordinary skill in the art to form ruthenium oxide capacitor lower electrode of RuOx as taught by Choi in the device formed by the

combination of Kunitomo et al. and Yeom et al. because ruthenium oxide such as RuOx is stable under the heat treatment during the process of forming the capacitor dielectric layer. Choi's col.1, lines 40-50.

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. view of Kotectki et al. (US 6,262,450).

Kunitomo et al. teaches all the limitations of claims 1, 3-4, 6, 8-9, 11, and 14-15 as shown above. Kunitomo et al. further teaches that the capacitor structure is formed as an element in a memory cell of a DRAM memory device, wherein the memory device further comprising: a row access circuitry (x0); a column access circuitry (EQ); a controller and an input/output circuit (Kunitomo et al.'s col.10, lines 39-41).

Kunitomo et al. does not explicitly teach that the memory device comprises an address decoder.

Kotectki et al. discloses a DRAM memory device comprises an address decoder. Kotectki et al.'s col.1, lines 30-39.

It would have been obvious to one of ordinary skill in the art to form the DRAM memory device including an address decoder as taught by Kotectki et al. because address decoder is commonly used to form in a peripheral region in order to support the memory device. Kotectki et al.'s col.1, lines 30-39.

Claims 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al. (US 5,815,427) in view of Kunitomo et al. (US 6,235,572).

Regarding claim 52, Cloud et al. discloses an electronic system comprising: a plurality of circuit modules (memory module, communication module, interconnection module) including a plurality of dies (a first die, a second die, and a third die), wherein the first die including an array of memory cells (10, a DRAM device. Cloud et al.'s abstract and col.4, lines 15-20); a plurality of leads (34, 26, 30) coupled to the plurality of dies to provide unilateral or bilateral communication and control; an user interface (video display, keypad and mouse. Cloud et al.'s col.6, lines 65-67). See Cloud et al.'s Fig.1, and Fig.7.

Cloud et al. does not explicitly teach that the DRAM memory device including an array of memory cells, wherein array of memory cells comprising: a capacitor structure including an insulator having a first compound which including substances, a conductive layer having a second compound including a first substance and a second substance, wherein the second substance in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer; at least one transistor having a gate, drain, and source, wherein the drain region is coupled to a second conductive layer.

Kunitomo et al. discloses a DRAM memory device including an array of memory cell, wherein the array of memory cells comprising: a capacitor structure including an insulator (61, a multi layered film including crystallized tantalum oxide films

56 and 58. Kunitomo et al.'s col.21, lines 55-60) having a first compound (tantalum oxide) which including substances (tantalum and oxygen) formed on a lower capacitor electrode (54); a conductive layer (53) with a uniform thickness having a second compound (ruthenium oxide) including a first substance (ruthenium) and a second substance (oxygen) is formed to prevent the oxygen (one substance of insulator layer) form the tantalum oxide (61) diffusing into plugs (49) (Kunitomo et al.'s col.18 lines 22-27 and col.21 lines 35-39); a transistor (Qs) having a gate (14A), a source (19) and a drain (19), wherein the drain (19) is coupled to a second conductive (30). See Kunitomo et al.'s Fig.26.

It would have been obvious to one of ordinary skill in the art to incorporate the DRAM memory device as taught by Kunitomo et al. into Cloud et al.'s electronic system because the capacitor structure and transistor structure of Kunitomo et al.'s DRAM memory has several advantages over conventional DRAM device as following: a capacity insulating film which has heat resistance, less leakage current and high withstand voltage; the film characteristics such as stress of capacity insulating film, surface morphology and density thereof have been improved; the effective film thickness of the transistor's gate insulating film is reduce and the generation of a tunneling is restricted; the performance of the DRAM concerning refresh characteristic has been improved.

Regarding claim 53, Cloud et al. teach the electronic system is formed in a computer system (80) which further comprising: a processor (44), a monitor (the video display); an output device (88) including a printer; bulk storage devices (90); data, and command buses. Cloud et al.'s Fig.7 and col.7, lines 1-15.

However, Cloud et al. does not explicitly teach that the computer system further comprises a memory controller, a plurality of data links and command links.

It would have been obvious to one of ordinary skill in the art to form the computer system including a memory controller, the data buses including data links, command buses including command signal and command links as claimed because these elements are art recognized elements which are commonly included in a computer system.

The limitations "as-deposited state" in claims 21, 24 and 51-53, "the trace amount of the third substance is oxidized during the crystallization of the dielectric" in claims 24 and 25 are taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et

al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Response to Arguments

3. Applicant's arguments with respect to claims 1-25 and 51-53 have been considered but are not persuasive.

Applicants argue that the applied arts do not teach the conductive layer is formed of a single layer. In responses, as above rejections, Kunitomo et al. and Lin et al. both teach the conductive layer formed of a single layer.

Conclusion

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

December 26, 2002